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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,945	04/17/2006	Katsumi Shibayama	46884-5451	8454

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EXAMINER	
LAM, CATHY N	

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
04/29/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/565,945	SHIBAYAMA, KATSUMI	
	Examiner	Art Unit	
	CATHY N. LAM	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) *1 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/17/2007, 01/26/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 32 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 1 and 8 are objected to because of the following informalities:

a) claim 1 recites the limitation of "the first superficial surface layer" in line 3; and the limitation of “the second surface layer" in line 5.

b) claim 8 recites the limitation of “ the second superficial surface layer “ in line 3.

There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) in view of Ootera (Pub # 2005/0265217 A1, published 12/01/2005).

Regarding claim1, AAPA fig. 32 shows a back illuminated photodetector comprising: a first conductive type semiconductor substrate 101; a second conductive type impurity semiconductor region 102 provided in the first superficial surface layer of the said semiconductor substrate; and a recessed portion (U shaped groove) for incidence of to-be-detected light formed in the second surface of the said semiconductor substrate and in an area opposite said impurity semiconductor region; and a window plate 113 provided on said surface to transmit said to-be-detected light to said coating layer. AAPA discloses all of the elements of the claims except a coating layer made of resin for transmitting said to-be-detected light to said recessed portion and having a substantially flat surface, said coating layer being provided on the second surface. In the same field of endeavor, Ootera discloses a coating layer 17/11 [0020,

0021] made of resin [0030] for transmitting said to-be-detected light to said recessed portion and having a substantially flat surface, said coating layer being provided on the second surface fig.1.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a coating layer made of resin for transmitting said to-be-detected light to said recessed portion and having a substantially flat surface, said coating layer being provided on the second surface, in order to undergo a change in properties when irradiated with a laser beam [0020].

Regarding claim 2, AAPA discloses the back illuminated photodetector according to claim 1. But AAPA does not disclose wherein said coating layer consists of a first resin layer provided on the second surface and second resin layer provided on said first resin layer and having a substantially fiat surface on the opposite side of said first resin layer, and wherein said first resin layer is arranged in such a manner that the portion provided on said recessed portion in the second surface is sunk lower than the portion provided on the outer edge portion of said recessed portion. In the same field of endeavor, Ootera discloses wherein said coating layer consists of a first resin layer 14 [0030] provided on the second surface and second resin layer 17 [0020] provided on said first resin layer 14 and having a substantially fiat surface on the opposite side of said first resin layer, and wherein said first resin layer is arranged in such a manner that the portion provided on said recessed portion in the second surface is sunk lower than the portion provided on the outer edge portion of said recessed portion fig.1.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a coating layer consists of a first resin layer provided on the second surface and second resin layer provided on said first resin layer and having a substantially fiat surface on the opposite side of said first resin layer, and wherein said first resin layer is arranged in such a manner that the portion provided on said recessed portion in the second surface is sunk lower than the portion provided on the outer edge portion of said recessed portion in order to undergo a change in properties when irradiated with a laser beam [0020].

Regarding claim 3, AAPA discloses the back illuminated photodetector according to claim 1 or 2, further comprising a supporting film (not labeled but on the first surface) provided on the first surface of said semiconductor substrate to support said semiconductor substrate fig.32.

Regarding claim 4, AAPA discloses the back illuminated photodetector according to claim 3, further comprising a filling electrode 105 penetrating through the supporting film and connected electrically to the impurity semiconductor region 103 at one end thereof fig.32.

Regarding claim 5, AAPA discloses the back illuminated photodetector according to claim 1 wherein said window plate 113 has a square cross-sectional shape with at least one comer being chamfered in a plane perpendicular to the thickness direction thereof fig.32.

5. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) in view of Ootera (Pub # 2005/0265217 A1, published 12/01/2005) further in view of Shibayama (US 2003/0218120, published 11/27/2003).

Regarding claim 6, AAPA/ Ootera disclose the back illuminated photodetector according to claim 1, except wherein a highly-doped impurity semiconductor region with impurities of said first conductive type added thereto at a high concentration is exposed across the entire side surface of said semiconductor substrate. In the same field of endeavor, Shibayama discloses wherein a highly-doped impurity semiconductor region with impurities of said first conductive type added thereto at a high concentration 1N [0103] is exposed across the entire side surface [0092] of said semiconductor substrate fig.10.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a highly-doped impurity semiconductor region with impurities of said first conductive type added thereto at a high concentration is exposed

across the entire side surface of said semiconductor substrate, in order to provide that any decline in image resolution in the connecting section to the detector can be suppressed [abstract].

Regarding claim 7, AAPA/ Ootera disclose the back illuminated photodetector according to claim 1, except wherein a highly-doped impurity semiconductor layer with impurities of the first conductive type added thereto at a high concentration is provided in the bottom portion of the recessed portion within the second superficial surface layer of the semiconductor substrate. In the same field of endeavor, Shibayama discloses a highly-doped impurity semiconductor layer with impurities of the first conductive type added thereto at a high concentration is provided in the bottom portion 1n' [0092] of the recessed portion (U shaped groove) within the second superficial surface layer of the semiconductor substrate fig. 10 (see the motivation as in claim 6).

Regarding claim 8, AAPA/ Ootera disclose the back illuminated photodetector according to claim 1, except wherein a highly-doped impurity semiconductor layer with impurities of said first conductive type added thereto at a high concentration is provided in the second superficial surface layer in the outer edge portion of said semiconductor substrate. In the same field of endeavor, Shibayama discloses a highly-doped impurity semiconductor layer with impurities of the first conductive type added thereto at a high

concentration is provided in the second superficial surface layer in the outer edge portion of said semiconductor substrate fig. 10 (see the motivation as in claim 6).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CATHY N. LAM whose telephone number is (571)270-5021. The examiner can normally be reached on M-F 7:30AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

CL
4/22/2008